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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,675	06/13/2001	Ghasi R. Agrawal	01-045	1803

7590 10/19/2004

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/880,675	AGRAWAL ET AL.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Amendment filed 6/17/2004, in reply to the Office Action mailed 3/1/2004. Claims 1-28 are still pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5,10-14 and 20-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Irrinki et al. (US 6067262) ISSUED: May 23, 2000.

Regarding independent Claims 1, 10, 20, Irrinki discloses an apparatus and method for a memory array (100, FIG. 1) employing a Built In-Self-Test and Repair circuit (BIST /BISR) 125, comprising a circuit BIST/BISR FLARESCAN register (120) for storing and protecting the address of the faulty memory location obtained in the built-in self repair (BISR) circuit 116, including:

An array of memory elements (array 100, FIG. 1) and a (BIST /BISR) circuit 125 for providing testing and soft repair of the memory element within the array (100). The FLARESCAN register comprises a plurality of soft latches such as "Flip-Flops", which are coupled together in series to form a BISR scan chain for storing the BISR repair information, controlled by the BISR circuit 116.

Providing a chip level scan enable signal (BIST_EN) FIG. 1, for enabling a scan test mode and a scan hold control signal (REGISTER CLOCK) for controlling the stored fault information in the soft latches "Flip-Flops" of the BISR FLARESCAN register, wherein the control signals (BIST_EN) and (REGISTER CLOCK) control the connection of the BISR scan chain to other scan chains during the scan test, so that the BISR repair information is held within the soft latches "Flip-Flops".

The BISR repair information is held within the soft latches of FLARESCAN register (120) and the scan test is part of a custom test flow employing a (BISR) circuit 116.

Regarding Claims 2-5, 11-14 and 21-24, Irrinki discloses (BIST EN) and (REGISTER CLOCK) signal, which prevent the BISR scan chain from being connected with other scan chains, by enabling each scan sequentially and for debugging the logic by scanning the BISR Scan signal at the input of the FLARESCAN register (120), which is the output error signal form the repair (BISR) circuit 116.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6, 15 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki et al. (US 6067262).

Regarding Claim 6, 15, 25, Irrinki does not specifically determine the expression for the test enable signal TE, wherein TE is the test enable signal, BS is the BISR scan signal, DE is the diagnose enable signal, CLSE is the chip level scan enable signal, and SHC is the scan hold control signal. However, the expression for the test enable signal is a logical expression, which is normally determined through well-known Boolean equations implemented with conventional digital logic or programmable memory techniques. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use well known Boolean equations in the apparatus and method of Irrinki, through conventional logic implementation for generating a logic level enable signal, since the BISR circuit comprises of digital logic circuitry which can be implemented accordingly, without the requirement of any extra hardware, to generate a desired logic signal.

4. Claims 7-9, 17-19 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki et al. (US 6067262) in view of Fosco et al. (US 6212656).

Regarding Claims 7-9, 17-19 and 26-28 Irrinki does not explicitly disclose BISR scan chain connected in a single scan chain separate from logic forming other scan chains, wherein the BISR scan chain is activated when required, wherein the BISR scan chain is multiplexed with a normal scan chain, wherein when the diagnose enable signal is low then the BISR scan chain is bypassed by the scan test and wherein when the diagnose enable signal is high, then the BISR scan chain is put in the scan test

path. Fosco et al. (US 6212656), in an analogous art, discloses in (FIG. 2) a method and apparatuses for testing of integrated circuit devices, including san-flops (12) electrically connected to each other in series to form a scan chain (20) for testing miscellaneous logic (24), where the data-in signal (DI) and the scan-in signal (SI) are input to MUX 14 selected by scan-enable signal (SE). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use scan chain (20) as taught by Fosco, with the BISR circuit of Irrinki, for the purpose of storing the fault signal representing a faulty memory location, so as to have a system and method for creating multiple scan chains having varying numbers of scan-flops, within a single design, while minimizing error rates and design time.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki et al. (US 6067262) in view of Hatada (US 6408414).

Regarding Claim 16, Irrinki does not explicitly disclose a scan hold control signal and diagnose enable signal provided by TAP controller. Hatada (US 6408414), in an analogous art, discloses (FIG. 8) a Test Access Port (TAP) controller 14, for controlling the overall operation of the Boundary-Scan test circuit and providing control signals to the scan chain. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ a (TAP) controller, as taught by Hatada, in the apparatus and method of Irrinki, for controlling operation of the Boundary-Scan test so a to sped up the testing of an electronic device.

Response to Arguments

6. Applicant's arguments filed 6/17/2004 have been fully considered but they are not persuasive. Claims 1-5,10-14 and 20-24 are rejected under 35 U.S.C. 102(b) and Claims 6, 15 and 25 are rejected under 35 U.S.C. 103(a) as being anticipated and as being unpatentable over Irrinki et al. (US 6067262). Claims 7-9, 17-19 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki et al. (US 6067262) in view of Fosco et al. (US 6212656). Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki et al. (US 6067262) in view of Hatada (US 6408414), as set forth in the present Office Action.

7. In response to Applicant's argument, page 10, that Irrinki fails to disclose, teach or suggest, the claimed limitations for "a scan test is any part of a custom test flow employing a BISR circuit" or " a scan test is part of a custom test flow", as amended in Claims 1, 10 and 20, as stated in the Office Action above, clearly Irrinki employs a (BISR) circuit 116 for implementing a scan test which is part of a custom test flow, and which is generally used for memory designs employing BISR, such as a memory array (100, FIG. 1) having a (BIST /BISR) circuit 125 for providing testing and soft repair of the memory element within the array (100).

8. Applicant argues, in reference to claims rejected under 35 U.S.C. 103(a), that Fosco, does not teach the elements of Claims 1, 10 and 20, and moreover Hatada does not disclose, teach, or suggest the elements of Claims 1, 10 and 20, since Hatada merely teaches a semiconductor device provided with a compact boundary scan test circuit.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, Fosco et al. (US 6212656), in an analogous art, discloses in (FIG. 2) a method and apparatuses for testing of integrated circuit devices, including san-flops (12) electrically connected to each other in series to form a scan chain (20). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the scan chain as taught by Fosco, with the BISR circuit of Irrinki, for the purpose of storing the fault signal representing a faulty memory location, so as to have a system and method for creating multiple scan chains having varying numbers of scan-flops, within a single design, while minimizing error rates and design time.

Further, Hatada (US 6408414), in an analogous art, discloses (FIG. 8) a Test Access Port (TAP) controller 14, for controlling the overall operation of the Boundary-Scan test circuit and providing control signals to the scan chain. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ a (TAP) controller, as taught by Hatada, in the apparatus and method of Irrinki,

for controlling operation of the Boundary-Scan test so a to sped up the testing of an electronic device.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
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Date: 12 October 2004
Office Action: Final Rejection

By: _____

JAMES C KERVEROS
Examiner
Art Unit 2133

GUY J. LAMARRE
PRIMARY EXAMINER